Amendments to the Specification:

Please replace paragraph [0021] with the following amended paragraph:

Please refer to Fig.2. Fig.2 is a schematic diagram of a wafer data figure 110 presented by the drawing step in Fig.1. In the present invention, the wafer data figure 110 displays a plurality of drawing files 114 according to a plurality of wafer data items 112. The wafer data items 112 include process time, wafer number, process step, and the wafer figure of each wafer. Each drawing file 114 uses a wafer figure icon 116 as a hyperlink to link with another displaying window to display the wafer figure of each wafer of the specific wafer data item 112 (drawing file of wafer defect distribution). Please refer to Fig.3. Fig.3 is a schematic diagram of the displaying screen 120 of the drawing file 114 in Fig.2. Each drawing file 114 uses a hyperlink to link with the displaying screen 120 through the wafer figure icon 116. The displaying screen 120 uses a wafer figure 122 to present a wafer defect distribution, uses a statistical figure 124 to present wafer defect statistical data, and uses a wafer data 126 to present a wafer data item 112 corresponding to each drawing file 114. The file size of the drawing file 114 is smaller than the file size of total amount of all wafer defect raw data corresponding to a wafer. For example, the drawing file 114 is able to be transferred as a compressed drawing file, such as a JPEG, to a terminal, and the terminal is able to decompress the compressed drawing file to present the drawing file on the displaying screen 120 to terminal users. Moreover, the displaying screen 120 is capable of displaying a plurality of wafer figures 122 simultaneously for allowing managers ~~mangers~~ to view the variation trend of each wafer defect distribution, and to allow managing engineers to compare and analyze each wafer defect distribution according to the specific wafer lot number and process step. For example, if defects gather in a specific corner on different wafers of the same lot number, it means that process step maybe has some

problems on the corner. In the other words, the present invention presents defect distribution figures of different wafers to assist managing engineers with quickly discovering the process possible problems in a macroscopic view.

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